ST. ANNE'S COLLEGE OF ENGINEERING AND TECHNOLOGY
(Approved by AICTE, New Delhi. Affiliated to Anna University, Chennai)
ANGUCHETTYPALAYAM, PANRUTI – 607 106.

QUESTION BANK

PERIOD: JULY 2023 – DEC 2023 **BATCH**: 2021 – 2025

BRANCH: ECE **YEAR/SEM:** III/V

SUBJECT: EC 3551 VLSI &CHIP DESIGN

UNIT – I - MOS TRANSISTOR PRINCIPLE

PART – A

1. Give the advantages of Integrated Circuit. [D]

- Size is less
- High Speed
- Less Power Dissipation

2. What is meant by CMOS technology? [D]

Complementary metal-oxide-semiconductor (CMOS) is a technology for constructing integrated circuits. CMOS technology is used in microprocessors, microcontrollers, static RAM and other digital logic circuits.

3. How do you construct MOS transistor? [D]

A Metal-Oxide-Semiconductor (MOS) structure is created by superimposing layers of conducting and insulating materials to form a structure.

4. What is meant by MOS transistor? [D]

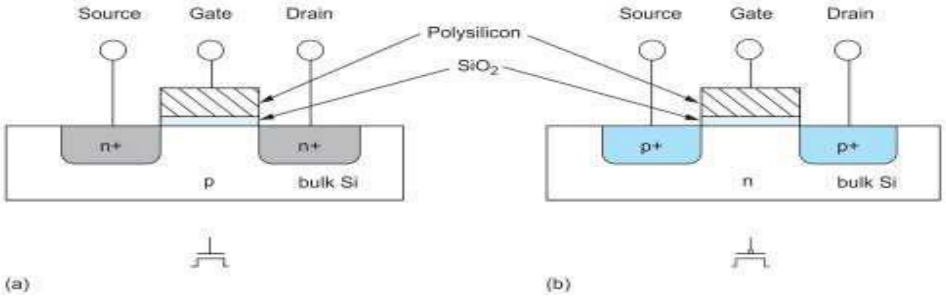
The transistor consists of a stack of the conducting gate, an insulating layer of silicon dioxide (SiO2) and the silicon wafer (also called the substrate, body, or bulk).

Gate of transistor is built from metal, so the stack is called metal oxide- semiconductor (MOS).Transistor operation is controlled by electric field so the device is also called Metal Oxide Semiconductor Field Effect Transistor (MOSFET).

5. What is a pull down device? (Nov 2009) [D]

A device is connected to pull the output voltage to the lower supply voltage (0V) is called pull down device.

6. Draw the schematic structure of n-MOS and p-MOS transistor with symbol. [D]



(a) n-MOS transistor (b) p-MOS transistor

7. What is a pull up device? [D]

A device is connected to pull the output voltage to the upper supply voltage usually V_{DD} is called pull up device.

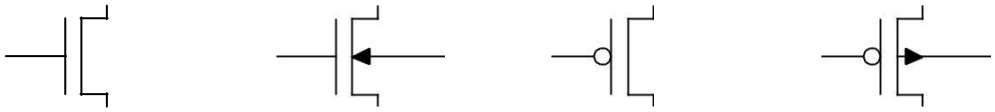
8. Compare nMOS and pMOS devices. (Nov 2007) [ID]

In nMOS, electrons are the majority carriers.

When the gate of an nMOS transistor is high, the transistor is ON. When the gate is low, then MOS transistor is OFF.

In pMOS, holes are the majority carriers. When the gate of a pMOS transistor is low, the transistor is ON. When the gate is high, then pMOS transistor is OFF.

nMOS Symbol pMOS Symbol



9. Compare depletion and enhancement mode devices. [Nov/Dec-2007] [D]

Depletion mode: The mode at which devices conduct with zero gate bias are called depletion mode.

Enhancement mode: The mode at which devices that are normally cut-off (i.e., non-conducting) with zero gate bias are called as enhancement mode.

10. Why nMOS technology is preferred more than pMOS technology? [ID]

The nMOS technology is preferred more than pMOS technology, because n- channel transistor has greater switching speed when compared to pMOS transistor

11. What is Moore's Law?[D]

The Moore's law states that number of transistor on an integrated circuit will double every 18 months.

12. What are the three types of modes of MOS transistor? (or) Give the different modes of operation of MOS transistor. (or) What are the different MOS layers? (Nov 2009) [D]

Three types of modes of MOS transistor are accumulation mode, depletion mode and inversion mode.

13. What is meant by accumulation mode in MOS transistor? [D]

If a negative voltage is applied to the gate, so there is negative charge on the gate. The positively charged holes are attracted to the region beneath (below) the gate. This is called the accumulation mode.

14. What is meant by depletion mode in MOS transistor? [D]

If a small positive voltage is applied to the gate, there are positive charges on the gate. The holes in the body are repelled from the region directly beneath (below) the gate, resulting in a depletion region forming below the gate.

15. What is meant by inversion mode (or) inversion layer in MOS transistor? [D]

If applying higher positive voltage exceeding a threshold voltage (Vt), attracting more positive charges to the gate. The holes are repelled and some free electrons in the body are attracted to the region beneath (below) the gate. This conductive layer of electrons in the p-type body is called the inversion layer.

16. List the different operating regions of MOS system. (May2012) [D]

Three operating regions of MOS transistor (or) system are

(i) Cut off region or sub threshold region
(ii) Linear region
(iii) Saturation region

17. When the channel is said to be pinched –off? (May 2010) [D]

If voltage between drain and source V_{ds} becomes sufficiently large that $V_{gd} < V_t$, the channel is no longer inverted near the drain and channel becomes pinched off.

Where V_g = gate-to-drain voltage, V_t= Threshold voltage.

19. When will nMOS transistor operates in cutoff region? [D]

If $V_{gs} < V_t$, the transistor is cutoff (OFF).

Where V_{gs} = gate-to-source voltage, V_t= Threshold voltage.

20. When will nMOS transistor operates in linear region? [D]

If $V_{gs} > V_t$, the transistor turns ON. If V_{ds} is small, the transistor acts as a linear resistor in which the current flow is proportional to V_{ds}.

Where V_{gs} = gate-to-source voltage, V_t= Threshold voltage & V_{ds}= drain-to-source voltage

21. When will nMOS transistor operates in saturation region? [D]

If $V_{gs} > V_t$ and V_{ds} is large, the transistor acts as a current source in which the current flow becomes independent of Vds .

Where V_{gs} = gate-to-source voltage, V_t= Threshold voltage & V_{ds}= drain-to-source voltage.

22. Determine whether an nMOS transistor with a threshold voltage of 0.7V is operating in the saturation region if V_{gs}= 2V and V_{ds}=3V.(Nov 2011) [D]

Condition for saturation region is $(V_{gs} – V_t) < V_{ds}$, So This nMOS transistor operated in the saturation region.

23. Give the expression for drain current (I_{ds}) for different modes of operation of MOS transistor. [D]

$$I_{ds} = \begin{cases} 0 & V_{gs} < V_t \quad \text{cutoff} \\ \beta\left(V_{gs} - V_t - V_{ds}/2\right)V_{ds} & V_{ds} < V_{dsat} \quad \text{linear} \\ \frac{\beta}{2}\left(V_{gs} - V_t\right)^2 & V_{ds} > V_{dsat} \quad \text{saturation} \end{cases}$$

24. List the different capacitances of a MOS transistor. [D]

Capacitances of a MOS transistor are

(i) Parasitic Capacitances or diffusion capacitances: C_{sb} (Source to body capacitance) & C_{db} (Drain to body capacitance)

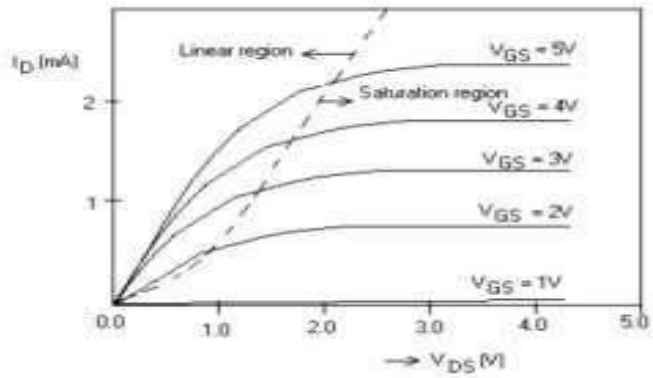
(ii) Intrinsic capacitance: The intrinsic capacitance has three components representing the different terminals connected to the bottom plate are C_{gb} (gate-to-body), C_{gs} (gate-to-source), and C_{gd} (gate-to-drain).

(iii) Overlap capacitance: C_{gsol} (overlap capacitance to the source) & C_{gdol} (overlap capacitance to the drain)

25. Define body effect (or) substrate bias effect. [May/June-2009] [Apr/may-2010] [D](OR)
What is meant by body effect? (NOV. 2014) [D](OR)Define body bias effect. (Nov 2016) [D]

Threshold voltage (V_t) is not constant with respect to voltage difference between substrate and source of the MOS transistor. This is known as body effect. It is otherwise known as substrate bias effect.

26. Draw the I-V characteristics of MOS transistor. (May 2012) [D]



27. What are the secondary effects (or) Non ideal effects of MOS transistor?[May2014] [D]

Secondary effects are

- Mobility degradation
- Velocity saturation
- Channel length modulation3+
- Body effect

- Subthreshold conduction
- Junction leakage current
- Tunneling
- Short channel effect

28. Define channel length modulation.(Nov 2011, April 2016, May 2017) [D]

Channel length modulation defines effective length of the conductive channel. It is modulated by the external applied Vds. Increasing Vds, causes the depletion region at the drain junction to grow and thus reduces the length of the effective channel.

29. What is body effect coefficient? (May 2011) [D] (Apr2021)

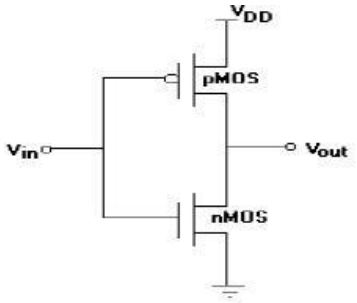
Body effect coefficient (γ) is

$$\gamma = \frac{t_{ox}}{\varepsilon_{ox}}\sqrt{2q\varepsilon_{si}N_A} = \frac{\sqrt{2q\varepsilon_{si}N_A}}{C_{ox}}$$

30. What do you mean by propagation delay time? (May 2017) [D]

Propagation delay time (t_{pd}) (or) Maximum delay is defined as maximum time from the input crossing 50% to the output crossing 50%.

31. Draw the circuit of a CMOS inverter. [D]



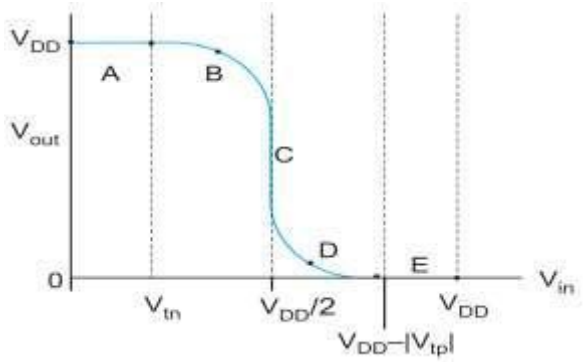
32. What are the advantages of CMOS inverter over the other inverter configurations? [D]

a. The steady state power dissipation of the CMOS inverter circuit is negligible.

b. The voltage transfer characteristic (VTC) exhibits a full output voltage wing between 0V and V_{DD}. This results in high noise margin.

33. Draw the DC transfer characteristics of CMOS inverter. (NOV.2013, APRIL-2015) [D]

DC transfer characteristics of CMOS inverter:



34. Define Noise margin. (May'13) [D]

Noise margin is the amount of noise that a CMOS circuit could withstand without affect the operation of circuit.

It is basically the difference between signal value and the noise value.

NM_L (NOISE MARGIN low) = V_{IL} - V_{OL}

NM_H (NOISE MARGIN high) = $V_{OH} - V_{IH}$

35. What are the steps involved in the process of IC fabrication? (May2010) [D]

Steps involved in IC fabrication:

- Silicon wafer Preparation
- Epitaxial Growth
- Oxidation
- Photolithography
- Diffusion
- Ion Implantation
- Isolation technique
- Metallization
- Assembly processing & Packaging

36. What are the different fabrication processes available to CMOS technology? [D]

P-well process, n-well process, Twin-tub process, and Silicon On Insulator (SOI)

37. What is threshold voltage? [D](Apr 2019)(Nov/Dec 2019)

The minimum voltage above which the MOSFET starts to conduct is known as threshold voltage.

38. List any two types of layout design rules. (Nov 2008, Nov 2009, May2010) [D]

Two types of layout design rules:

a. Lambda design rules
b. Micron rules

39. What are design rules? (OR)

What is the need for design rules? (NOV.2014) [D]

Design rules are a set of geometrical specifications that dictate the design of the layout masks. Design rules are used to produce workable mask layouts from which the various layers in silicon will be formed or patterned.

40. Define the lambda layout rules. (May 2013) What is meant by lambda layout design rules?

Discuss any two layout design rules. (MAY 2014, APRIL2015, Nov 2015, Nov 2008, Nov 2009, May 2010) [D]

Lambda-based rules are round up dimensions of scaling to an integer multiple of scalable parameter λ. Lambda rules make scaling layout as small. The same layout can be moved to a new process by specifying a new value of λ.Micron rules can result in as much as a 50% size reduction over lambda rules. Industry usually uses the micron design rules for layouts.

41. What are stick diagrams? [D]

Stick diagrams are used to convey layer information through the use of a color code. A stick diagram is a cartoon of a chip layout. The stick diagram represents the rectangles with lines which represent wires and component symbols.

42. What are the uses of Stick diagram? [D]

- It can be drawn much easier and faster than a complex layout.

- These are especially important tools for layout built from large cells.

43. Give the various color coding used in stick diagram. [D]

Various color coding used in stick diagram:

- Green – n-diffusion, Red- polysilicon, Blue –metal, yellow- implant and Black- contact areas.

44. Why does interconnect increase the circuit delay? [Nov/Dec-2011] [D]

Interconnect is defined by its resistance value and capacitance with neighbor. Delay is calculated from resistance and capacitance value.

45. What is transistor sizing problem?(MAY 2014) [D]

Transistor sizing is carried out by equating the maximum on resistances of the logic circuit with inverter one.

46. What is CMOS latchup? How do you prevent Latch up problem? (Nov 2008) (or) What is Latch up problem in CMOS circuits? (May 2008, April 2016) [D]

Latch up is a condition in which the parasitic components give rise to the establishment low resistance conducting paths between V_{DD} and V_{SS} with disastrous results.

Careful control during fabrication is necessary to avoid this problem.

The remedies for the latch-up problem include:

(i) An increase in substrate doping levels.
(ii) Reducing Rnwell.
(iv) By introducing guard rings.
(v) By introducing SOI (Silicon On Insulator)

47. What is BiCMOS Gate? [D]

Compare CMOS and BiCMOS technology. (NOV. 2013) [D]

When bipolar and MOS technology are merged, the resulting circuits are referred to as biCMOS circuits. It improves bandwidth and current gain.

48. What do you mean by lateral scaling? [ID]

Lateral spacing in process of scaling the separation region between interconnect layers, keeping thickness t_{ox}, length and width as constant value.

49. What is meant by scaling? [Nov/Dec-2013, April 2018] [D]

Scaling is reducing feature size of transistor. The transistor size has reduced by 30% every two to three years. As transistors become smaller, they switch faster, dissipate less power, and are cheaper to manufacture.

50. List different types of scaling. (NOV./DEC. 2014) [APRIL-2015] [D]

Types of scaling are transistor scaling and interconnect scaling.

Types of transistor scaling are lateral scaling, constant field scaling and constant voltage scaling.

51. What are the advantages of scaling? [APRIL-2015] [D]

Advantages of scaling are better reliability, reducing complexity and reducing IC size.

52. What is the influence of voltage scaling on power and delay? [Apr/May-2011] [D]

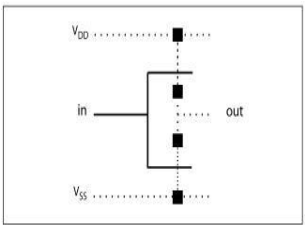
Due to voltage scaling, the power dissipation will be reduced with the increase in delay (i.e) speed decreases.

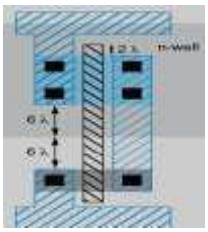
53. What is the need of demarcation line? (Nov 2017) [D]

In CMOS, a demarcation line is drawn to avoid touching of p-diff with n-diff. All pMOS must lie on one side of the line and all nMOS must lie on other side.

54. Draw the stick diagram and layout for CMOS inverter. (Nov 2016, April 2018) [D]

Stick diagram **Layout diagram**





55. What are simulations available for VLSI circuits?

In VLSI the following simulations are available

- Path simulation, Monte Carlo simulation and Interconnect simulation

56. Why nMOS transistor is selected as pull down network? (Nov 2017) [D](OR)
Why nMOS conducts strong zero and weak one? [D](Nov 2018)

Pull-up and pull-down networks in CMOS circuits are never both conducting and are never both opened at the same time. This is the reason that **nMOS** transistors are used in the **pull-down** network and pMOS in the **pull-**up network of a CMOS gate.

57. By what factor gate capacitance must be scaled if constant electric field is to be applied. (Nov 2015) [ID](Apr 2019)

Constant voltage scaling is increasing the electric fields in devices.

Voltage scaling has dramatically slowed down due to leakage. This may ultimately limit CMOS scaling.

58. Define SSI, MSI, LSI and VLSI. (May 2009) [D]

Small-Scale Integration (SSI) circuits have less than 10 gates. Example: 7404 inverter.

Medium-Scale Integration (MSI) circuits have up to 1000 gates. Example: 74161 counter.

Large-Scale Integration (LSI) circuits have up to 10,000 gates. Example: 8-bit microprocessor (8085).

Very large scale Integration (VLSI) with gates counting up to 1 lakh. Example: 16-bit microprocessor

59. Give objective of layout design rule. [D]

The main objective of the layout rule is to build reliably functional circuits in as small area as possible.

60. What is velocity saturation effect? (April 2018) [D]

In MOSFET operation, at high Electric field strength the velocity charge carriers gets reduced (saturated), which in turn reduces the current flow Ids.This is known as velocity saturation.

61.What is meant by RC delay model? [D]

RC delay model approximates the nonlinear transistor I-V and C-V characteristics with an average resistance and capacitance over the switching range of the gate.

62. Draw equivalent RC delay model for a MOS transistor? [D]

Equivalent RC delay model for an nMOS and pMOS transistor:

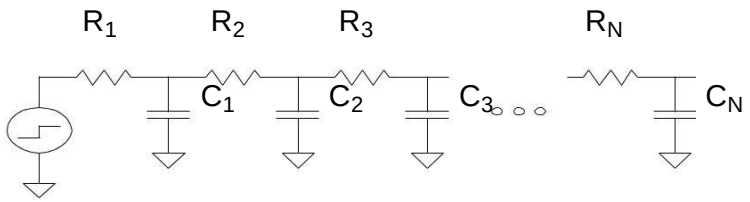
63. What is Elmore's delay model? (or) Give the expression for Elmore delay and state the various parameters associated with it. (NOV. 2014, April 2016, April 2017, Nov 2017, April 2018,MAY2021) (D)

The Elmore delay model estimates the delay from a source switching to one of the leaf nodes. Delay is summing over each node i of the capacitance C_i on the node multiplied by the effective resistance R.

Propagation delay time:

$$= R_1C_1 + (R_1 + R_2)C_2 + ... + (R_1 + R_2 + ... + R_N)C_N$$

RC delay equivalent for series of transistors:



64. Define logical effort and give logical effort value of inverter. [D]

Logical effort (g) is defined as the ratio of the input capacitance of a gate to the input capacitance of an inverter delivering the same output current.

An inverter has a logical effort of 1.

65. Write the general expression of logical effort for n inputs NAND and NOR gate? [D]

Expression of logical effort for n inputs NAND is (n+2)/3.

Expression of logical effort for n neither inputs NOR is (2n + 1)/3. Where, n – no. of inputs.

66. Define electrical or fanout. [D]

Electrical effort is defined as ratio of the output capacitance to input capacitance of a gate.

Electrical effort (h) = C_{out} / C_{in}

67. What is parasitic delay? [D]

The parasitic delay (P) of a gate is the delay of the gate when it drives zero load. It can be estimated with RC delay models.

68. Write the general expression of parasitic delay for n inputs NAND and NOR gate. [D] (Apr2022)

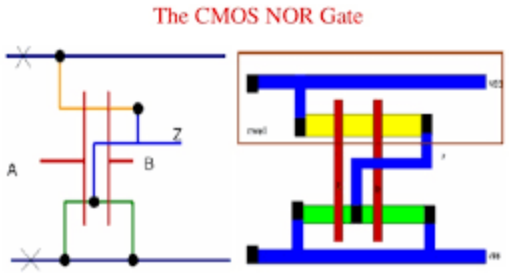
Expression of parasitic delay for n inputs NAND and NOR is n. Where, n – no. of inputs.

69. Write an expression for the logical effort and parasitic delay of n input NOR gate. [Nov/Dec-2011] [D]

Logical effort for n inputs NOR gate is (2n+1)/3

Parasitic delay for n inputs NOR gate is n

70. Draw the stick diagram for CMOS NOR gate.(Nov/Dec 2019)(Nov/Dec 2022)



PART – B
[First Half]

[MOS TRANSISTOR PRINCIPLE-I]

1. Explain the basic concept of nMOS and pMOS transistor with relevant symbol. (16) **[D] (Apr2021)**

2. Explain the accumulation mode, depletion layer and inversion layer of MOS transistor with diagram.(16) **[D]**

3. Discuss the cutoff, linear and saturation region operation of MOS transistor. **(Nov 2009,2018) [D]**

4. Explain in detail about the ideal I-V characteristics of a NMOS and PMOS device. (**Apr2023) (MAY 2013,2018) [D]** **(OR)**

Discuss in detail with necessary equations the operation of MOSFET and its current-voltage characteristics. **(April/May 2011, May 2016). [D] (OR)(Apr 2019)**

Derive drain current of MOS device in different operating regions. **(Nov/Dec 2014)(May/June 2013) (Nov 2012, Nov 2016) [D] (OR)**

Explain in detail about the ideal I-V characteristics and non-ideal I-V characteristics of a NMOS and PMOS device**. (May/June 2013) [D]**

5. Discuss the CV characteristics of the CMOS. **(Nov 2012, May 2014, Nov 2015, Nov 2016, April2018) [D]**
(OR)

Explain the electrical properties CMOS**. (Nov 2017). [ID]**

6. Explain the DC transfer characteristic of CMOS inverter**.[APRIL-2015, Nov 2015] [D] (Apr 2019) (Apr2021)**

(Nov/Dec 2011) (Nov/Dec 2012) (May/June 2013) (April/May 2012) (May/June 2014) (Nov/Dec 2013) (May 2016, May 2017, Nov 2008) [D] (Nov 2007, Nov 2009) (Nov/Dec 2022) [D] (Apr2022,2023)

7. Explain in detail about the non ideal I-V characteristics of a CMOS device. **[D]**

8. Explain in detail about THRESHOLD effect in MOS device. **[D]**

9. Discuss the scaling principles and its limits. **(MAY 2013, Nov 2017, 2018) [D] (Nov 2012, Dec 2011, Nov 2015, May 2016) [D](May 2017) [D] (Nov/Dec 2019)**

[MOS TRANSISTOR PRINCIPLE-II]

10. Explain about stick diagram in VLSI design. **(April 2008) [D] (Apr 2019)**

11. Draw and explain briefly the n-well CMOS design rules. **(NOV 2007, April 2008, MAY 2014) [D]**

12. Write the layout design rules and draw diagram for four input NAND and NOR. **(Nov 2016, 2017, April2018) [D] (Apr 2019)**

13. Derive expressions for the drain-to-source current in the non saturated and saturated regions of operation of an nMOS transistor. **(Nov 2007, Nov 2008) [D]**

14. Briefly discuss about the classification of circuit families and comparison of the circuit families. (May 2014, April-2015, April 2018) **(ID)**

15. What is meant by skewed gate and give functions of skewed gate with schematic diagrams?

16. What is meant by Elmore's delay and give expression for Elmore's delay?

17. Explain Pass transistor logic with neat sketches. (April 2008, April2018) **(ID) (Apr 2019) (Apr2022)**

18. Discuss in detail the characteristics of CMOS Transmission gates. (May 2016, May 2017, Nov 2017, 2018) **(D) (Apr 2019)**

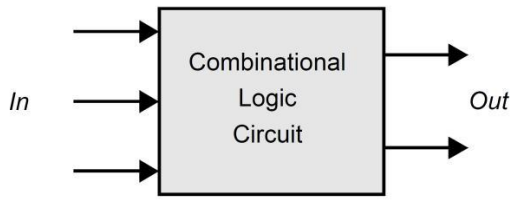
19. Write short notes on ratioed circuits. (Nov 2016) **(D)**

UNIT – II - COMBINATIONAL LOGIC CIRCUITS

PART – A

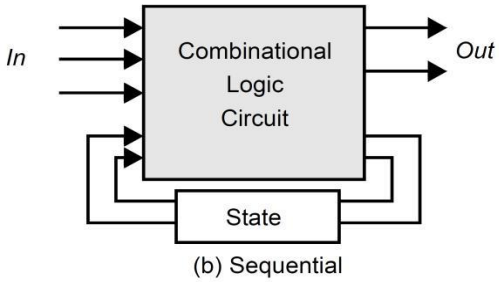
1. Define combinational circuit and give an example. [D]

A combinational circuit can be defined as a circuit, whose output is dependent only on the inputs. Example: full adder.



2. Define sequential circuit and give an example. [D]

A sequential circuit can be defined as a circuit, whose output depends not only on the present value of its inputs but on the sequence of past inputs. Example: flip-flop.



(b) Sequential

3. What is the static CMOS inverter? [D]

Static CMOS inverter circuit is the combination of nMOS pulldown and pMOS pullup network.

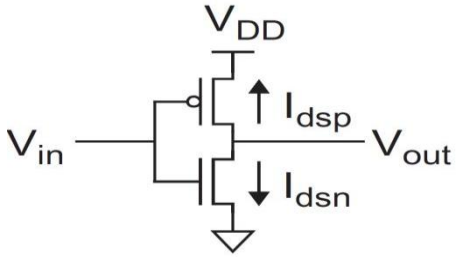


Figure: Static CMOS inverter

4. What are the advantages of static CMOS circuits? [ID]

Advantages of static CMOS circuits are

- Static CMOS circuits have good noise margins
- Static CMOS circuits are fast, low power, easy to design.
- Static CMOS circuits are widely supported by CAD tools,
- Static CMOS circuits are available in standard cell libraries.

5. What are the disadvantages of static CMOS circuits? [ID]

Disadvantages of static CMOS circuits are

It requires both nMOS and pMOS transistor on each input.

It has large logical effort.

Gate delay is increased.

6. What is bubble pushing? (May 2010) [D]

- A NAND gate is equivalent to an OR of inverted inputs.

- A NOR gate is equivalent to an AND of inverted inputs.
- The same relationship applies to gates with more inputs.
- Switching between these representations is easy and is often called bubble pushing.

7. What is meant by compound gate? [D]

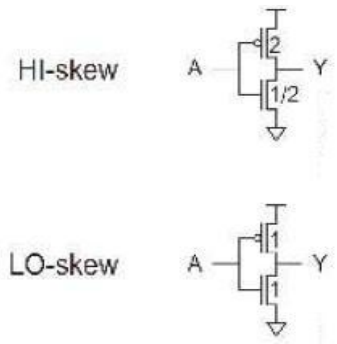
Static CMOS efficiently handles compound gates computing various inverting combinations of AND/OR functions in a single stage.

8. What is the function of skewed gate? [D]

One input transition is more important than the other. HI-skew gates to favor the rising output transition and LO-skew gates to favor the falling output transition.

9. What are the types of skewed gate? [D]

Two types of skewed gate are HI-skew gate and LO-skew gate.



10. Define P/N ratio. [D]

P/N ratio is defined as the ratio of pMOS to nMOS transistor width. For processes, a mobility ratio of $\mu n/\mu p = 2$.

11. What is meant by ratioed logic? [D]

In ratioed logic, a gate consists of an nMOS pull-down network that realizes the logic function and a simple load device, which replace the entire pull-up network.

12. What is meant by pseudo nMOS logic? [D]

A pseudo nMOS logic (ratioed logic) which uses a grounded pMOS load is referred to as a pseudo nMOS gate.

13. Draw a pseudo nMOS inverter.(Nov 2011) [D]

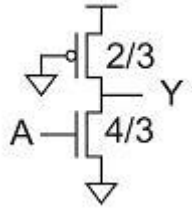


Figure: Pseudo nMOS inverter

14. What are the disadvantages of using a pseudo nMOS gate instead of a full CMOS gate?(May 2012) (D)(OR)

What is the drawback of pseudo nMOS logic? [ID]

- Pseudo-nMOS gates will not operate correctly if (Maximum low level output) VOL >VIL (Maximum low level input) of the receiving gate.
- Ratioed circuits dissipate power continually in certain states and have poor noise margin.
- Ratioed circuits used in situations where smaller area is needed.

15. What are advantages and disadvantages of ratioed logic? [D]

Advantage: Stronger static loads produce faster rising outputs.

Disadvantages:

a. Degrade the noise margin and burn more static power when the output is 0.
b. A resistor is a simple static load, but large resistors consume a large layout area in typical MOS processes.

16. Compare CMOS combinational logic gates with reference to the equivalent nMOS depletion load logic with reference to the area requirement.(May 2012) [D]

For CMOS, the area required is 533μm^2, for pseudo nMOS the area required is 288 μm^2

17. What is AOI logic function? [D]

AND OR Invert logic function (AOI) implements operation in the order of AND, OR, NOT operations. So this logic function is known as AOI logic function.

18. What is AOI 221 Gate? [D]

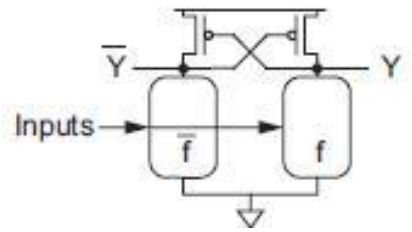
AOI 221, here 221 refers to number of inputs in each section.

19. What is meant by Asymmetric Gates? [D]

When one input is far less critical than another, even nominally symmetric gates can be made asymmetric to favor the late input at the expense of the early one.

20. What is meant by Cascode Voltage Switch Logic? [D]

Cascode Voltage Switch Logic (CVSL) seeks the benefits of ratioed circuits without the static power consumption. It uses both true and complementary input signals and computes both true and complementary outputs using a pair of nMOS pulldown networks.



21. What are the advantages of Cascode Voltage Switch Logic? [D](OR)

State the reasons for the speed advantages of CVSL family. (Nov 2012)

Advantage: CVSL has a potential speed advantage, because all of the logic is performed with nMOS transistors, thus reducing the input capacitance.

22. Define rise & fall time. [April 2008, Nov/Dec-2008] [Nov/Dec-2009] (D)

Rise time (tr):

- It is defined as time for a waveform to rise from 20% to 80% of its steady state value. Fall time (tf):
- It is defined as time for a waveform to fall from 80% to 20% of its steady-state value.

23. What is edge rate? [D]

Edge rate is defined as an average value of rise time and fall time.

Edge rate (t_{rf}) = (t_r + t_f)/2

24. What do you mean by propagation delay time? [D]

Propagation delay time (tpd) (or) Maximum delay is defined as maximum time from the input crossing 50% to the output crossing 50%.

25. What do you mean by contamination delay time? [D]

Contamination delay time (tcd) (or) Minimum delay is defined as minimum time from the input crossing 50% to the output crossing 50%.

26. What is meant by average contamination delay time? [D]

Average contamination delay time ($\mathbf{t_{cd}}$) is defined as an average value of rising contamination delay time ($\mathbf{t_{cdr}}$) and falling contamination delay time ($\mathbf{t_{cdf}}$).

Contamination delay time (t_{cd}) = (t_{cdr} + t_{cdf})/2

27. What is meant by dynamic logic? [D]

α. Dynamic logic using a clocked pull up transistor rather than a pMOS that is always ON.

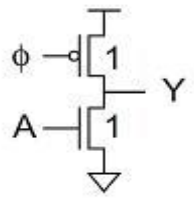


Figure: Dynamic logic

28. What are the two modes of operation in dynamic logic and give its functions? [D]

Dynamic circuit operation has two modes, as shown in Figure.

a. During precharge, the clock ϕ is 0, so the clocked pMOS is ON and output Y is high.

b. During evaluation, the clock is 1 and the clocked pMOS turns OFF. The output may remain high or may be discharged low through the pulldown network.

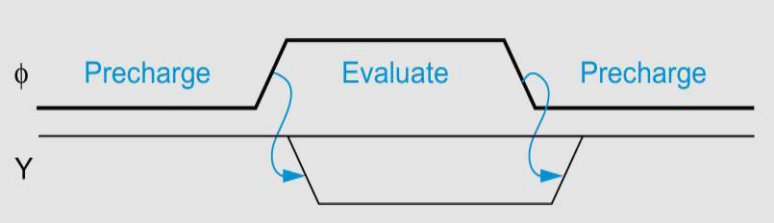


Figure: Precharge and evaluation of dynamic gates

29. What are the disadvantages of dynamic Logic? [D]

The disadvantages of dynamic logic are
- Dynamic circuits require careful clocking.
- Dynamic circuits consume significant dynamic power.
- Dynamic circuits are sensitive to noise during evaluation mode.
- Monotonicity problem
- Dynamic circuits suffer from charge leakage.

30. What are the advantages of dynamic logic? [D]

The advantages of dynamic logic are
- Dynamic circuit has lower input capacitance and no contention during switching. • Zero static power dissipation.

31. What is the use of footed transistor in dynamic logic circuit? [D] Nov/Dec 2022
How will you add charge sharing problem?

An extra clocked evaluation transistor can be added to the bottom of the nMOS stack to avoid contention as shown in the below figure. The extra transistor is called a foot.

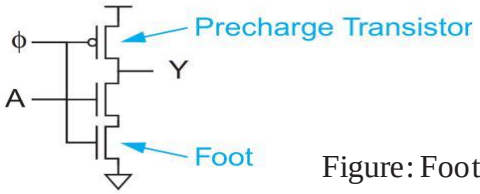


Figure: Footed dynamic inverter

32.What is meant by Monotonicity problem? [D]

During precharge, the output is pulled HIGH. When the clock rises, the input is HIGH, so the output is discharged LOW through the pull down network. The input later falls LOW, turning OFF the pull down network.
However, the precharge transistor is also OFF, so the output floats, staying LOW rather than rising. This is called Monotonicity problem in dynamic circuit.

Figure: Monotonicity problem

33. What is meant by domino logic? [D]

The Monotonicity problem can be solved by placing a static CMOS inverter between dynamic gates. This converts the monotonically falling output into a monotonically rising signal. The dynamic-static pair together is called domino logic.

34. Write the features of CMOS dominoLogic? [D]

Features of CMOS Domino Logic are

α. These structures occupy small area.
β. Parasitic capacitance is to be small to increase the speed.
χ. Each gate can make one logic"1" to logic 0 transitions.

35. What is the use of keeper circuit? [D]

The keeper is a weak transistor that holds or *staticizes* the output at the correct level when it floats.

36. What is meant by pass transistors? [D]

In pass-transistor circuits, inputs are applied to the source/drain diffusion terminals. A single nMOS or pMOS pass transistor suffers from a threshold drop.

37. Which MOS can pass logic 1 and logic 0 strongly? [D]

p-MOS can pass strong logic 1.

n-MOS can pass strong logic 0.

38. What is meant by CMOS Transmission gate? (Nov 2007, May 2011)(Or) [D]
Define Transmission gate. (May 2009) (Apr2022)

A parallel pair of nMOS and pMOS transistors is called *transmission gate*.

Transmission gates solve the threshold drop problem but require two transistors in parallel.

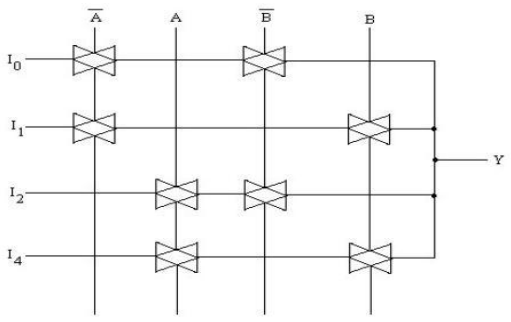
39. State the advantages of Transmission gate. (April 2017) [D] (Apr2021)

Transmission gates solve the threshold drop problem.

It provides good conducting path between input and output.

40. Draw the CMOS implementation of 4-to-1 MUX using transmission gates. [D](Apr 2019) Nov/Dec 2022(Apr2021)

CMOS implementation of 4-to-1 MUX using transmission gates:



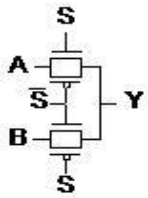
41. What are the various forms of inverter based CMOS logic? [D]

Various forms of inverter based CMOS logic:

Pseudo nMOS logic
Dynamic CMOS logic
Clocked CMOS logic
CMOS domino logic

42. Draw 2:1 MUX using transmission gate. (Nov 2008, APRIL-2015, 2016) [D]

2:1 MUX using transmission gate:

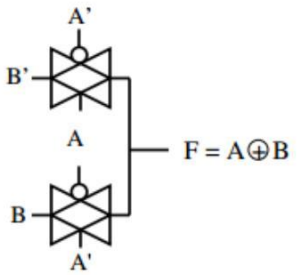


43. Draw XOR and XNOR using transmission gates. [Apr/may-2010] [D] (Nov/Dec 2019)

- **2 I./P XOR using TGs:**

F = A.B' + A'.B , we need this: if A=1 → F = B' (pass B' to F)
if A=0 → F = B (pass B to F)

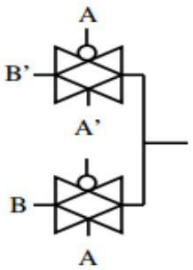
using TGs:



8 Ts (2 inverters for A and B and two TGs)
Versus 12 Ts for regular CMOS

2 I/P XNOR

F = A.B + A'B' if A=1 → pass B to F
if A=0 → pass B' to F



44. Define power dissipation. [Nov/Dec-2013] (D)

Power dissipation is defined as power consumed by the transistor unnecessarily, therefore increasing the power requirement to the logic.

45. List the types of power dissipation. [APRIL 2015, Nov 2017] (OR) List the various power losses in CMOS circuits. (May 2013,April 2018) (D)(Apr 2019) (Apr2022)

Types of power dissipation are static and dynamic power dissipation

46. Compare static & dynamic power dissipation? [D](Nov/Dec 2019) (Apr2021)

Dynamic power dissipation is power consumed by transistor when it operates.

At some stage both transistor pMOS and nMOS are in ON stage which, leads to short circuit formation between V_{DD} and GND, thus unwanted power dissipation occurs.
Static power dissipation is power consumed by transistor when it is not in operating stage.

47. What do you mean by low power design? [D]

When both static and dynamic powers are reduced then, the circuit is said to be low power designed circuit.

48. What are the factors that cause dynamic power dissipation in CMOS circuits? List the sources of dynamic power consumption. (Nov 2016) (D)

Dynamic dissipation due to charging and discharging load capacitances as gates switch.

"Short-circuit" current while both pMOS and nMOS stacks are partially ON.

49. How can dynamic power dissipation reduced? (or) [D]

State any two criteria for low power logic design. (Nov 2015, MAY 2014) (D)

Dynamic power dissipation ($P_{dynamic}$) expressed as below,

$$P_{dynamic} = \alpha C V_{DD}^2 f$$

To reduce dynamic power, use the following

- α: clock gating, sleep mode
- C: small transistors (esp. on clock), short wires
- V_{DD}: lowest suitable voltage
- f: lowest suitable frequency

50. Write the expression for power dissipation in CMOS inverter. [Nov/Dec-2008] (D)

Total power dissipation P_{total} is the sum of dynamic power dissipation ($P_{dynamic}$) and static power dissipation (S_{tatic}).

$P_{total} = P_{dynamic} + S_{tatic}$

Where, $P_{dynamic} = \alpha C V_{DD}^2 f$

- α:activity factor
- C: capacitor
- V_{DD}: Supply voltage
- f: Supply frequency

$$P_{static} = (I_{sub} + I_{gate} + I_{junc} + I_{contention}) V_{DD}$$

51. What are the factors that cause static power dissipation in CMOS circuits? [Nov-2012] (D) (OR) List the sources of static power consumption. (Nov 2016) (D)

Static dissipation occurs due to

Sub threshold leakage through OFF transistors
Gate leakage through gate dielectric
Junction leakage from source/drain diffusion
Contention current in ratioed circuits

52. How can static power dissipation reduced? [D]

- Selectively use ratioed circuits

- Selectively use low V_t devices
- Leakage reduction: Use stacked devices, body bias and low temperature.

53. Why single phase dynamic logic structure cannot be cascaded? Justify.(May 2016) (D)

No, single phase dynamic logic structure cannot be cascaded. Because monotonicity problem will be raised, so static logic should be used in between dynamic logics structure.

54. What is Complementary Pass Transistor logic? (NOV/DEC-2014) (D)

Complementary Pass Transistor logic has complementary data inputs and outputs.
It reduces the count of transistors used to make different logic gates, by eliminating redundant transistors.

55. Give the effects of supply voltage and temperature variations CMOS circuits. [Nov-2012] (D)

(ι) Supply voltage may vary due to tolerance of voltage regulators, IR drop along the supply rail and di/dt noise.

(ιι) Typically the supply is specified as +/- 10% around nominal (uniform distribution).

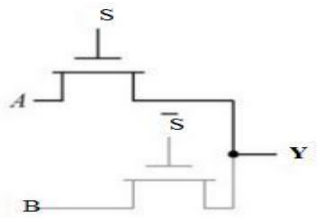
(ιιι) Speed is proportional to VDD, also noise budgets are affected.

Temperature

Parts must operate over a range of temperatures.

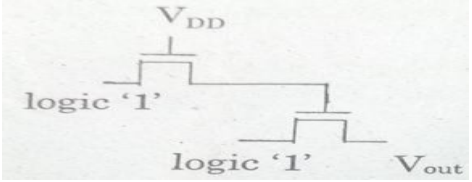
Standard	*Minimum*	*Maximum*
Commercial	0°C	70°C
Industrial	-40°C	85°C
Military	-55°C	125°C

56. Implement a 2:1 multiplexer using pass transistor. (NOV/DEC-2013, April 2015) [D]



57. What is the value of V_{out} for the figure shown below, where V_{tn} is threshold voltage of transistor? (Nov 2016) (D)

Output voltage, $V_{out} = V_{DD}-2V_{tn,}$ Where V_{tn} : Threshold voltage



PART – B

[COMBINATIONAL CIRCUITS-I]

1. Explain the detail about pseudo-nMOS gates with neat circuit diagram. (April/May 2011)(Nov/Dec 2013). **(D)**

2. Implement NAND gate using pseudo- nMOS logic. (Nov 2013,April 2018) **(D) (Apr2022)**
3. Explain about DCVSL logic with suitable example. (May 2017) **(D) (Apr2022)**
4. Describe the basic principle of operation of dynamic CMOS, domino and NP domino logic with neat diagram. (NOV 2011, 2016) **(D) (Nov/Dec 2022)**

5.(i) Suppose we wish to implement F=A+B+C and G=A+B+C+D.Assume both true and complementary signals are available. Implement these functions in dynamic CMOS stages to reduce the transistor count.

(ii) What logic function is implemented in the above logic.To which logic family does the circuit belong? Does the circuit have any advantages over fully complementary CMOS.(Nov/Dec 2019)

PART – B
[First Half]
[COMBINATIONAL CIRCUITS-II]

5. Explain the domino logic families with neat diagrams. (NOV 2012, APRIL-2015, Nov 2017) **(D) (Apr2021)**

6. Explain the keeper logic family **or** signal integrity issue with neat diagrams. **(**April 2018, Nov 2018**)(ID)**

7. Describe the basic principle of operation of NP domino logic. (NOV 2011) **(D) (Apr2021)**

8. Explain the components of static and dynamic power dissipation in CMOS circuits with necessary diagrams and expressions. (DEC 2011, Nov 2015, NOV 2016, May 2017, May 2010) (Nov 2012, May 2013, Nov 2014, May 2016). Compare static and dynamic power.(D) **(Apr 2019) (Nov/Dec 2019) (Apr2021)**

9. Implement the following expression Y'=AB+ACE+DE+DCB in static CMOS logic function using no more than 10 transistors.(Nov/Dec 2019) (D)

10. Explain various ways to minimize the static and dynamic power dissipation. (Nov 2013, May2015) **(D)**

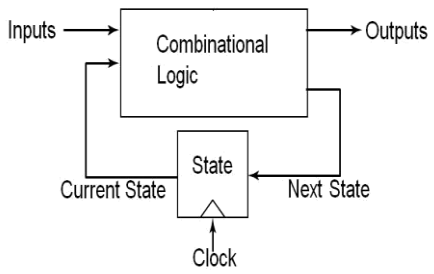
11. Discuss the low power design principles in detail. (Nov 2017). **(D)**

UNIT-III SEQUENTIAL LOGIC CIRCUITS

PART – A

1. What is a Sequential circuit?

In sequential circuits, the output depends on previous as well as current inputs.



2. What are sequencing methods available in sequential circuit design? (NOV/DEC-2012) (D)

The sequencing methods available in sequential circuit design are,

Flip-flop
Two phase transparent latches
Pulsed latches

3. What is meant by maximum delay or setup time failure and how to avoid?

If the combinational logic delay is too high, the receiving element will miss its setup time and sample the wrong value. This is called a *setup time failure* or *max-delay failure*. Max-delay can be solved by redesigning the logic to be faster or by increasing the clock period.

4. Define sequencing overhead.

Sequencing overhead is defined as an additional delay to Tokens (Data) that are already critical, decreasing the performance of the system. This extra delay is called sequencing overhead.

5. What is meant by Min-delay failure and how to avoid?

If the hold time is large and the contamination delay is small, data can incorrectly propagate through two successive elements on one clock edge, corrupting the state of the system. This is called a race condition, hold-time failure, or min-delay failure.

Min-delay can only be fixed by redesigning the logic, not by slowing the clock.

6. Define time borrowing. (Apr2021)

Time borrowing is defined as if one half-cycle or stage of a pipeline has too many logics; it can borrow time into the next half-cycle or stage. Time borrowing can accumulate across multiple cycles.

7. What is the clock skew? (April 2018)(April 2019) (Apr2022)

Clocks have some uncertainty in their arrival times that can cut into the time available for useful computation.

8. How to design CMOS flip-flop?

Dynamic inverting flip-flop built from a pair of back-to-back dynamic latches.

9. How to design Semi dynamic Flip-flop?

Klass-semidynamic flip-flop (SDFF) is a cross coupled between a pulsed latch and a flip-flop.

10. What is meant by semi dynamic flip-flop (SDFF)?

The SDFF accepts rising inputs slightly after the rising clock edge. Like a flip-flop, falling inputs must set up before the rising clock edge called as *semi dynamic*. It combines the dynamic input stage with static operation.

11. What is meant by Differential flip-flop?

Differential flip-flops accept true and complementary inputs and produce true and complementary outputs. They are built from a clocked sense amplifier so that they can respond to small differential input voltages.

12. What is meant by True Single Phase Clock (TSPC) Latch or flip-flop?

True Single Phase clock Latch or flip flop avoids complementary clock pulse.

13. What are sequencing dynamic circuits?

Sequencing dynamic circuits are

i. Traditional domino circuit

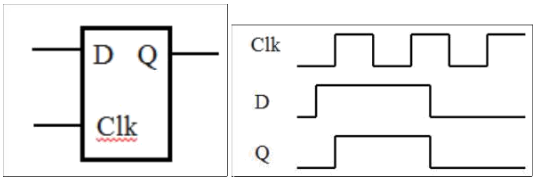
Ii.Skew tolerant domino circuit

14. Define Synchronizer. (MAY/JUE-2014)

Synchronizer is defined as a circuit that accepts an input that can change at arbitrary times and produces an output aligned to the synchronizer's clock.

15. What is a Latch? (NOV/DEC-2014)

Latch is a bistable device. i.e., it has two stable states (0 and 1). It is the level triggering method.



16. What is a flip-flop? (NOV/DEC-2014)

Flip-flop is a bistable device. i.e., it has two stable states (0 and 1). It is the edge triggering method.

17. What is meant by Bistability? (Apr2022)

A latch is a bistable device. i.e., it has two stable states (0 and 1). Latch can enter a metastable state in which the output is at an indeterminate level between 0 and 1.

18. Define aperture.

Aperture is defined as a setup and hold time around the rising edge of the clock.

19. How to design simple synchronizer circuit.

Simple synchronizer built from a pair of flip-flops. *F*1 samples the asynchronous input *D*. The output *X* may be metastable for some time, but will settle to a good level with high probability.

20. What is meant by Arbiter?

The *arbiter* is closely related to the synchronizer. It determines which of two inputs arrived first.
If the spacing between the inputs exceeds some aperture time, the first input should be acknowledged.
If the spacing is smaller, exactly one of the two inputs should be acknowledged, but the choice is arbitrary.

21. What are the advantages of differential Flip flop? (Nov 2011) (D)

The advantages of differential Flip flops are

Reduce the parasitic delay of the pull down networks.
Lower electric fields across the pull down networks.
It reduces the channel length of the transistors.

22. State the reasons for the speed advantages of CVSL family. (Nov 2012, Nov 2014) (D)

CVSL has a potential speed advantage because all of the logic is performed with nMOS transistors, thus reducing the input capacitance.

23. Enumerate the features of synchronizers. (May 2013) (D)

a. A good synchronizer should have a feedback loop with high gain bandwidth product.
b. It can produce metastable output.

24. What are the disadvantages of using a pseudo nMOS gate instead of a full CMOS gate? (May 2012) (D)

Ratioed circuits dissipate power continually in certain states and have poor noise margin than complementary circuits. Ratioed circuits used in situations where smaller area is needed.

25. What is Klass-semidynamic flip-flop?

Klass-semidynamic is a single-input single-output positive edge-triggered flip-flop.

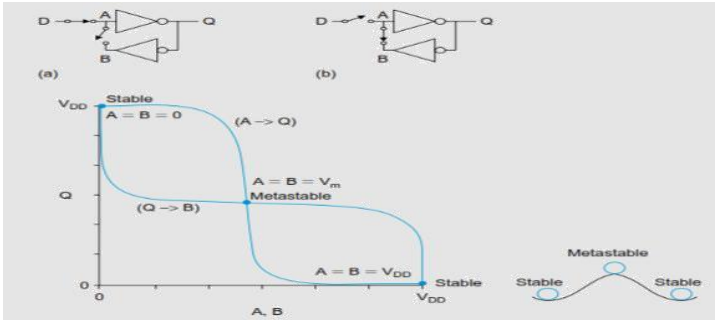
It is domino-style from end allows for efficient embedded combinational logic and reduces the load on the data network.

26. What are the different phases of VLSI design flow?

The different phases of VLSI design flows are**,**

Function Verification and testing, logic synthesis/Timing verification
Logical verification and testing
Floor planning automatic place and route
Layout verification
Implementation

27. Draw the circuit diagram of a CMOS bistable element and its time domain behavior. (APRIL/MAY-2011) (D)



28. What is CMOS clocked SR flip-flop? [D]

CMOS Clocked SR flip-flop consists of a cross-coupled inverter pair, plus 4 extra transistors to drive the flip-flop from one state to another and to provide clocked operation.

29. What do mean by multiplexer based latches? [D]

Multiplexer based latches can provide similar functionality to the SR latch, but has the important added advantage that the sizing of devices only affects performance and is not critical to the functionality.

30. What is Master-Slave Based Edge Triggered Register? [D]

The register consists of cascading a negative latch (master stage) with a positive latch (slave stage).

31. What is the advantage of multiplexer based latch? [D]

The advantage of the multiplexer-based register is the feedback loop is open during the sampling period, and sizing of devices is not critical to functionality.

32. What is pseudo static? [D]

The register employs a combination of static and dynamic storage approaches depending upon the state of the clock.

33. What is called Clocked CMOS Register? (May 2016) (D)

C^2MOS is a positive edge-triggered register based on the master-slave concept which is insensitive to clock overlap. The register operates in two phases.

34. What is meant by Dual-edge Triggered Register? Give it advantage. [ID]

Dual-edge triggered register is a design of sequential circuits that sample the input on both edges. The advantage of this scheme is that a lower frequency clock.

35. What is True Single-Phase Clocked Register (TSPCR)? [ID]

The True Single-Phase Clocked Register (TSPCR) uses a single clock (without an inverse clock).

36. What is the advantage and disadvantage of True Single-phase clocked register? [D]

The main advantage is the use of a single clock phase. The disadvantage is the increase the number of transistors. 12 transistors are required.

37. What is pipelining? (Dec. 2016, April 2017) (D)

Pipelining is a popular design technique used to accelerate the operation of the datapaths in digital processors.

38. What is necessary of non-overlapping clocks? [D]

The non-overlapping of the clocks ensures correct operation. When CLK and *CLK* signals are non-overlapping, correct pipeline operation is obtained.

39. What is topology for NORA-CMOS?(Nov 2017) (D)

The latch-based pipeline circuit implemented using C^2MOS latch is known as NORA-CMOS circuit. A NORA CMOS circuit is race-free as long as all the logic functions between the latches are non-inverting.

40. Tabulate the operation modules of NORA-CMOS circuit. [D]

	CLK block		$\overline{CLK}$ block	
	Logic	**Latch**	**Logic**	**Latch**
CLK = 0	Precharge	Hold	Evaluate	Evaluate
CLK = 1	Evaluate	Evaluate	Precharge	Hold

41. Define the dynamic-logic rule. [D]

Inputs to a dynamic CLKn (CLKp) block are only allowed to make a single 0 $\rightarrow$ 1 (1 $\rightarrow$ 0) transition during the evaluation period.

42. Define C^2MOS design rule. [D]

C^2MOS design rule is defining to avoid races, the number of static inversions between C^2MOS latches should be even.

43. Draw the switch level schematic of multiplexer. (May 2016) [D]

.

44. What is known as H-tree clock distribution? [D]

The H-tree configuration is useful for regular-array networks in which all elements are identical and the clock can be distributed as a binary tree. For example, arrays of identical tiled processors.

45. Define clock jitter. (Nov 2017) [D]

Clock jitter refers to the temporal variation of the clock period at a given point. i.e, the clock period can reduce or expand on a cycle-by-cycle basis.

46. What is meant by Latch based clocking? [D]

Use of registers in sequential circuits enables a robust design methodology. Advantage is combinational logic is separated by transparent latches

47. Compare synchronous and asynchronous design. (April 2017) [D]

Synchronous design	Asynchronous design
Synchronous logic is both faster and simpler.	Asynchronous logic is slow and complex.
Distributing a clock at high speed becomes exceedingly difficult.	Distributing a clock at high speed becomes easy.

48. Differentiate between latch and flip-flop registers. (Nov 2015) (D)(April 2018)(ID)(Nov/Dec 2019) (Apr2021)

Latch is a bistable device. i.e., it has two stable states. It is the level triggering method. Flip-flop is a bistable device. i.e., it has two stable states. It is the edge triggering method. Register has set of flip fops.

49. Define setup and hold time. (Nov/Dec 2019)

The setup time is the interval before the clock where the data must be held stable.

The hold time is the interval after the clock where the data must be held stable. Hold time can be negative, which means the data can change slightly before the clock edge and still be properly captured. Most of the current day flip-flops has zero or negative hold time.

50. State the uses of Schmitt trigger. (Nov/Dec 2022)

The function of the Schmitt trigger is to convert any regular or irregular shaped input waveform into a square wave output voltage or pulse.

PART-B

[SEQUENTIAL CIRCUITS-I]

1. Discuss in detail various static latches and registers. (Nov 2016) **(D) (OR) (Apr2021)**

Explain the methodology of sequential circuit design of Latches. (May 2014) **(OR)**

Discuss the operation of a CMOS latch. (Nov 2007) **(D)**

2. Explain the operation of master-slave based edge triggered register. (May 2016, April2018) **(Nov/Dec 2019) (D)(Nov/Dec 2022,May 2023) (OR)**

Draw and explain the operation of conventional CMOS, pulsed and resettable latches. **(D)** (Nov 2012, 2018).

3. Discuss about the design of sequential dynamic circuits. (Nov 2012, Nov 2017) **(D) (OR)**

Explain the methodology of sequential circuit design of flip-flop. (May 2014) **(D)**

4.Design a d-flip-flop using transmission gate. (Nov 2016) **(D) (Apr 2019)**

5. Explain the operation of True Single Phase Clocked Register. (Nov 2016, April 2017) **(D)**

6. Explain in detail about timing issues needed for a logic operation. (April 2017). (Nov 2017, 2018) **(ID)**

7. Explain in detail about pipelining structure needed for a logic operation. (April 2017, Nov 2017) Nov/Dec 2021(D) (OR) **(Apr2022) (Apr2021)**

Discuss in detail various pipelining approaches to optimize sequential circuits. (May 2013, 2016) **(D)**

8. Discuss about the NORA–CMOS structure. (Nov 2016) **(D)**

9. Explain the clock distribution techniques in synchronous design in detail. (Nov 2017, April2018) **(D)**

10.Discuss about asynchronous design in logic design.

PART-B

[SEQUENTIAL CIRCUITS-II]

11. How do eliminates metastability problem in sequential circuit and explain? **(D)**

12. Compare synchronous and asynchronous design. **(D)**

13. Explain briefly about sense amplifier based registers and pulse registers. **(D) (Nov/Dec 2022,May 2023) (Apr2021)**

14. Explain about Monostable and Astable Sequential Circuit in VLSI. **(D) Nov/Dec 2022 (Apr2021) (Apr2022)**

15. Explain about Schmitt trigger Circuit in VLSI. **(D) (Apr2022)**

UNIT-IV (DESIGNING OFARITHMETIC BUILDING BLOCKS AND SUBSYSTEM)

PART-A

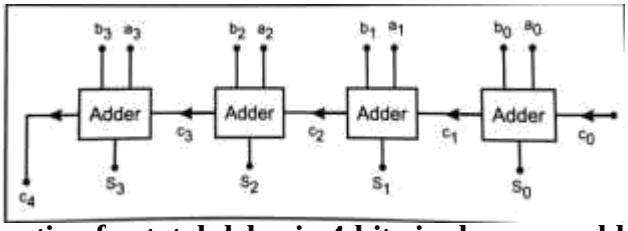
1. What is meant by data path circuits? (APR 2016) [D]

Data path circuits are meant for passing the data from one segment to other segment for processing or storing.
The data path is the core of processors, where all computations are performed.

2. What is ripple carry adder? [D]

If n bits are added, then we can get n-bit sum and carry of C_n. C_i= Carry in bit from the previous column. N bit ripples carry adder needs n full adders with C_{i+1} carry out bit.

3. Draw the circuit for 4 bit ripple carry adder.(Nov 2018) [D]



4. Write the equation for total delay in 4 bit ripple carry adder. [ID]

The total delay using the following equation,

$t_{4b} = t_d (c_{in} \rightarrow S_3) + 2t_d (c_{in} \rightarrow c_{out}) + t_d (a_0, b_0 \rightarrow c_1)$

5. Write the equation for worst case delay in 4 bit ripple carry adder. [D]

If it is extend to n-bit, then the worst case delay is

$t_{n\text{-}bit} = t_d (c_{in} \rightarrow S_{n-1}) + (n-2)t_d (c_{in} \rightarrow c_{out}) + t_d (a_0, b_0 \rightarrow c_1)$

6. What is meant by carry Look ahead Adder (CLA)? [ID]

A carry-look ahead adder (CLA) or fast adder is a type of adder used in digital logic.

A carry-look ahead adder improves speed by reducing the amount of time required to determine carry bits.

The carry-look ahead adder calculates one or more carry bits before the sum, which reduces the wait time to calculate the result of the larger value bits.

7. Write the general expression for carry signal in CLA.(ID)(April 2018) [ID]

We can write carry look-ahead expressions in terms of the generate gi and propagate pi signals. The general form of carry signal ci thus becomes

$c_{i+1} = a_i . b_i + c_i . (a_i \oplus b_i) = g_i + c_i . p_i$, If $a_i . b_i$ =1, then c_{i+1} = 1,

8. Write the equation for generating term in CLA. [D]

In the case of binary addition, A + B generates if and only if both A and B are 1. If we write G (A, B) to represent the binary predicate that is true if and only if A + B generates, write generate term as, $g_i = a_i . b_i$

9. Write the equation for propagates term in CLA. [D]

In the case of binary addition, A + B propagates if and only if at least one of A or B is 1. If we write P(A,B) to represent the binary predicate that is true if and only if A + B propagates, we have: Write the propagate term as, $p_i = a_i \oplus b_i$

10. What are the two factors that Carry look ahead adder depends on? [D]

Carry look ahead depends on two things: Calculating, for each digit position, whether that position is going to propagate a carry if one comes in from the right. Combining these calculated values to be able

to deduce quickly whether, for each group of digits, that group is going to propagate a carry that comes in from the right.

11. Write the generalized equation for CLA. [D]

$$S_i = P_i \oplus c_i$$
$$c_1 = g_0 + P_0.c_0$$
$$c_2 = g_1 + P_1.c_1 = g_1 + P_1.(g_0 + P_0c_0)$$
$$c_3 = g_2 + P_3.c_3$$
$$c_3 = g_3 + P_3.c_3$$
$$= g_3 + P_3.g_2 + P_3.P_2.g_1 + P_3.P_2.P_1.g_0 + P_3.P_2.P_1.P_0.C_0$$

12. Name the limitations of MODL. [ID]

- MODL has following limitations as

i. clocking in mandatory

ii. The output is subject to charge leakage and charge sharing.
iii. Series connected nFET chains can give long discharge times.

13. What is called Manchester Carry Chain Adder? [D]

The Manchester carry chain is a variation of the carry-lookahead adder that uses shared logic to lower the transistor count.

As seen in CLA implementation section, the logic for generating each carry contains all of the logic used to generate the previous carries.

A Manchester carry chain generates the intermediate carries by tapping off nodes in the gate that calculates the most significant carry value.

14. Write the basic equation for Manchester Carry Chain Adder? [D]
Write about kill, propagate, generate term in CLA. (Apr 2019)

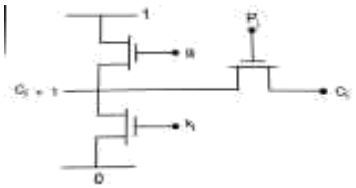
In this adder, the basic equation is $c_{i+1} = g_i + c_i . p_i$

Where $p_i = a_i \oplus b_i$ and $g_i = a_i . b_i$

Carry kill bit $k_i = a_i + b_i = a_i . b_i$
f K_i=1, Hence,
k_i is known as carry kill bit

15. Draw the switch level circuit for Manchester carry chain adder. [D]

The switch level circuit is given as



16. What are high (wide) adders? [D]

The adders with more than 4 bits can be designed. This is known as wide or high speed adders. Brute-force approach can be used to design 8 bit adder.

17. What are the types of high speed adders? [D]

Types of high speed adders are

1. Carry Skip adder
2. Carry Select adder
3. Carry Save adder.

18. What is Carry skip adder? [D]

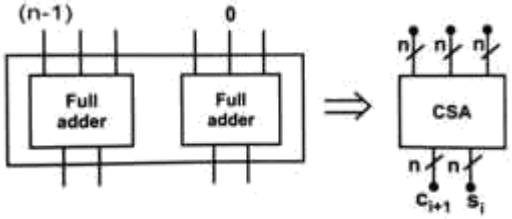
- Carry skip adder is one of the high speed adder.
- When BP= $P_0P_1P_2P_3$ =1, the incoming carry is forwarded immediately to the next block.
- Hence the name carry bypass adder or carry skip adder.
- Idea: if (P_0 and P_1 and P_2 and P_3 =1) the $C_{03} = C_0$, else "kill" or "generate".

19. What is Carry Select adder?
Write the principle of any one fast multiplier. (NOV 2016) [D]

- Adding two n-bit numbers with a carry-select adder is done with two adders in order to perform the calculation twice.
- After the two results are calculated, the correct sum, as well as the correct carry-out, is then selected with the multiplexer once the correct carry-in is known.

20. What is Carry save adder? [D]

- In carry save adder, the carry does not propagate. So, it is faster than carry propagate adder.
- It has three inputs and produces 2 outputs, carry-out is saved. It is not immediately used to find the final sum value.



n-bit Carry Save Adder

21. What are accumulators? [D]

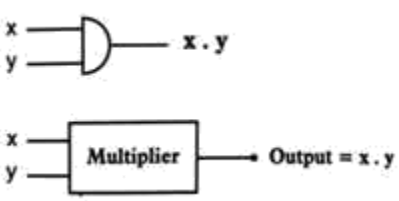
- Accumulator acts as a part of ALU and it is identified as register A. The result of an operation performed in the ALU is stored in the accumulator.
- It is used to hold the data for manipulation (arithmetic and logical)

22. What are multipliers? [D]

- Multiplier is used in computation process, which multiplies two binary numbers.
- Basic operations in multiplication are given below.
  0 x 0 = 0, 0 x 1 = 0, 1 x 0 = 0, 1 x 1 = 1

23. Draw the truth table of multiplier. [D]

The truth table of multiplier is



x	y	x . y
0	0	0
0	1	0
1	0	0
1	1	1

24. Mention the steps involved in multiplying by shifting. [D]

If x=(0020)2 = (2)10 If it is to be multiplied by 2, then we can shift x in left side. • If it is to be divided by 2, then we can shift in right side. So, shift register can be used for multiplication or division by 2.

25. Write the delay equation for array multiplier. [D]

The equation for array multiplier is

$$P_i = \sum_{i=j+k} x_j y_k + c_{i-1}$$

$$P = X.Y = \left(\sum_{j=0}^{n-1} x_j 2^j\right)\left(\sum_{k=0}^{n-1} y_k 2^k\right) = \sum_{i=0}^{n-1}\sum_{j=0}^{n-1}\left(x_j y_k 2^{j+k}\right)$$

26. What is meant by divider circuit? [D]

Divider circuit is used in arithmetic operation in digital circuits. Dividing is carry out by repeated subtraction and addition.

27. What are the types of dividers available in VLSI? [D]

There are two types of dividers. They are serial divider and parallel divider.

28. Compare serial divider and parallel divider. [D]

Serial divider is slow and parallel divider is fast in performance. Array divider is fast compared with the serial divider. But hardware requirement is increased.

29. What is shift register? [D]

An n-bit rotation is specified by using the control word $R_{0\text{-}n}$ and L/R bit defines a left or right shifting.
For example y3 y 2 y 1 y 0 = a3 a2 a1 a0
If it is rotated 1-bit in left side, we get y3 y 2 y 1 y 0 = a2 a1 a0 a3
If it is rotated 1-bit in right side, we get y3 y 2 y 1 y 0 = a0 a3 a2 a1

30. What is meant by Barrel shifter? (April 2018) [D]State the merits of by Barrel shifter.(Nov/Dec 2019)

A barrel shifter is a digital circuit that can shift a data word by a specified number of bits in one clock cycle.

It can be implemented as a sequence of multiplexers (MUX). The output of one MUX is connected to the input of the next MUX in a way that depends on the shift distance.

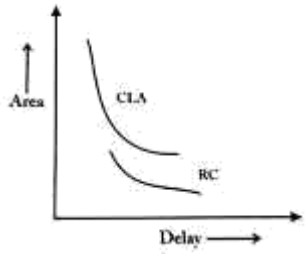
31. What is the area constraint between carry look ahead adder and ripple carry adder? [D]

The area of a carry look ahead adder is larger than the area of a ripple carry adder. Carry look ahead adder are parallel, which requires a larger number of gates and also results in a larger area.

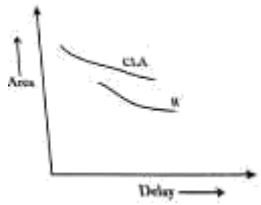
32. What is the drawback of carry look ahead adder? [D]

In the carry look ahead adder, need large area because computations are in parallel and more power is consumed.

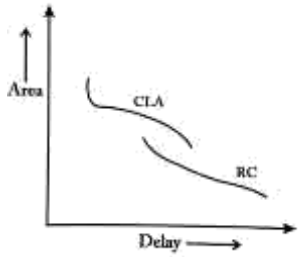
33. Draw the graph between area Vs delay of carry lookahead and ripple carry adder for 8 bit. [D]



34. Draw the graph between area Vs delay of carry lookahead and ripple carry adder for 16 bit. [D]



35. Draw the graph between area Vs delay of carry lookahead and ripple carry adder for 32 bit. [D]



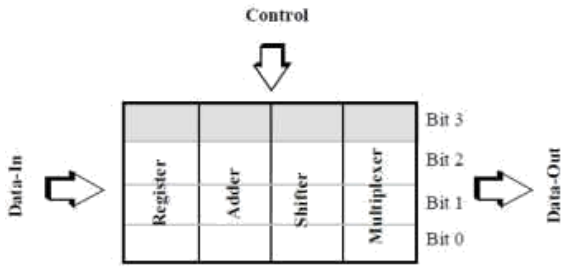
36. What is meant by bit – sliced data path organization? (May 2016) [D]

Data paths are arranged in a bit sliced organization, instead of operating on single bit digital signals.

The data in a processor are arranged in a word based fashion. Bit slices are either identical or resemble a similar structure for all bits.

37. Draw and list out the components of data path. (May 2017) [D]

Data path block consists of arithmetic operation, logical operation, shift operation and temporary storage of operands.



38. Determine propagation delay of n-bit carry select adder. (May 2016) [D]

Propagation delay, P of n-bit carry select adder is equal to $\sqrt{2}$ where N = N- bit adder

39. Mention the application of Barrel shift register. [D]

Why is barrel shifter very useful in the designing of arithmetic circuits? (NOV 2016) [D]

- A common usage of a barrel shifter is in the hardware implementation of floating-point arithmetic.
- For a floating-point add or subtract operation, requires shifting the smaller number to the right.
- This is done by using the barrel shifter to shift the smaller number to the right by the difference, in one cycle.

40. What is latency? (Nov 2017) [D]

Clock latency (or clock insertion delay) is defined as the amount of time taken by the clock signal in traveling from its source to the sinks.

41. Give the applications of high speed adder. (May 2017) [D]

CMOS high speed adder adders used in processor, data processing application and data path application with low power consumption.

42. What is meant by booth multiplier? [D]What is radix 2 algorithm? (Apr2019)

Booth's algorithm is an efficient hardware implementation of a digital circuit that multiplies two binary numbers in two's complement notation.
Booth multiplication is a fastest technique that allows for smaller, faster multiplication circuits, by recoding the numbers that are multiplied.

43. What is meant by array multiplier? [D]

- Array multiplier uses an array of cells for calculation.
- Multiplier circuit is based on repeated addition and shifting procedure. Each partial product is generated by the multiplication of the multiplicand with one multiplier digit.
- N-1 adders are required where N is the number of multiplier bits.

44. What is Wallace tree multiplier? And give its advantages. [ID] (Apr2021)

The Wallace tree multiplier output structure is tree basis style. It reduces the number of components and reduces the area.

45. How to design a high speed adder? (Nov 2017) [D]

Design of high speed adder is done using CMOS and transmission gates in submicron.

Design of high speed adder is done using parallel adder manner.

46. What are parameters used to characterize the memory? [D] (Apr2021)

Parameters used to characterize a memory device are area, power and speed.

47. How can you classify memory based on operation mode? [D]

Classifications of memory based on operation mode are 1. ROM, 2. RAM

48. How can you classify memory based on data storage mode? [D]

Classifications of memory based on data storage mode are 1. Volatile, 2. Non-volatile

49. Define ROM. Give some examples. [D]

ROM is a memory where code is written only one time. Examples are washing machine, calculator, games etc.

50. What are advantage and disadvantages of programming ROM? [D]

Advantage: basic cell only consists of transistor. No need of connection to any of the supply voltage.

Disadvantage: As it has pseudo nMOS, it is ratioed logic and consumes static power

51. What is meant by non-volatile memory? [D] (Apr2022)

Non-volatile consists of array of transistors. These are placed on a word line – bit line grid. We can write the program by enabling or disabling these devices selectively.

52. What is floating gate transistor? [D]

Floating gate transistor is mostly used in all the reprogrammable memories. In floating gate transistor, extra polysilicon strip is used in between the gate and the channel known as floating gate.

53. What is EPROM and Flash EPROM? [D]

Erasing is done by passing UV rays on the cell by using transparent window. This process will take some seconds to some minutes.

Flash ROM is a combination of density of EPROM and versatility of EEPROM. Avalanche hot electron injection mechanism is used here. Erasing can be done by Fowler-Nordheim tunneling concept. Erasing is done in bulk.

54. What is RAM? And give types of RAM. [D]

RAM is read and write memory. Types are static and dynamic RAM.

55. Distinguish Static and dynamic RAM. [D] Nov/Dec 2022

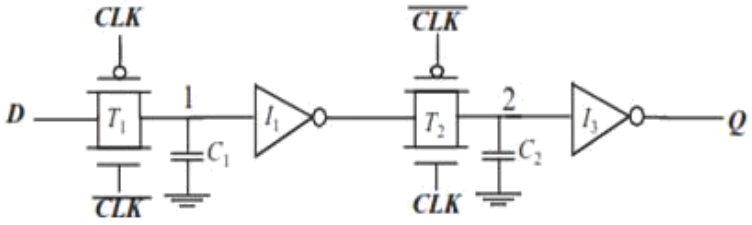
SRAM:

SRAM cell needs 6 transistors per bit. Bit line (BL) and inverse Bit Line signals are used to improve the noise margin during read and write operations.

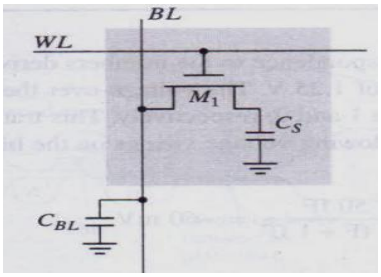
Dynamic RAM:

Content in the cell can be periodically rewritten through a resistive load, called as refresh operation. Here cell content is read follow by write operation.

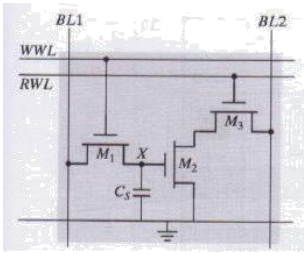
56. Draw the schematic of dynamic edge –triggered register. (Dec. 2016) (D)



57. Design a one transistor DRAM cell. (Nov 2013, April 2015) (D)(Apr 2019) Nov/Dec 2022(Apr2022)



58. Design a three transistors DRAM cell.[D]



59. Mention the different hardware architectures used for multipliers. (Nov/Dec 2019)

AND gate, Adder, Shifters

PART-B

[FIRST HALF]

1. Discuss about data path circuits. **[D]**
2. Draw the structure of ripple carry adder and explain its operation. (Nov 2017) **[D]**

How the drawback in ripple carry adder overcome by carry look ahead adder and discuss. (Nov 2017,2016,May 2017) (April 2018)(ID) **(Apr 2019) (Apr2022)**

3. Discuss about Manchester Carry Chain Adder. **[D]**
5. Discuss about different types of high speed adders. (Apr. 2016, 2017, May 2016) **[D]**
6. Design a carry select adder and discuss its features. (May 2016) **[D]**

PART-B
[SECOND HALF]

7. Briefly discuss about ALU.
8. Explain the design and operation of 4 bit unsigned array multiplier circuit and Wallace multiplier circuit. (Apr. 2016, Nov 2016, May 2017, 2018). **[D] (Apr 2019) (Nov/Dec 2019) Nov/Dec 2022**
9. Explain in detail about Radix 4,radix 2 Booth multipliers. **[D] (Apr 2019) (Nov/Dec 2019) Nov/Dec 2022(Apr2022) (Apr2021)**
10. Discuss about shifter and 4 Bit barrel shift adder.(Nov 2018) **[D] (Nov/Dec 2019) Nov/Dec 2022**
11. Discuss the details about speed and area trade off. (May 2017) **[D] (Apr2022)**
13. Discuss Memory classification and its architecture and building blocks. **[D] (Nov/Dec 2022)**
14. Discuss Memory core its types in detail. (April 2018) **[D]**
15. Explain about Low power static RAM and dynamic RAM.(Nov 2018) **[D] (Apr 2019) (Nov/Dec 2019) (Apr2022)**
16. Explain about CAM. **[D]**
17. Discuss about Low power memory design. **[D] (Nov/Dec 2019)**

UNIT-V (IMPLEMENTATION STRATEGIES AND TESTING)

PART-A

1. What is Routing? [D]

Once the designer has floor planned a chip and the logic cells within the flexible blocks have been placed, it is time to make the connections by routing the chip.

2. What are the types of routing and what is Global Routing? (April2018) (Nov 2018) [ID]

There are two types of routing. Global and Hierarchical routing. A global router does not make any connections, it just plans them. We typically global route the whole chip before detail routing the whole chip (or the pieces).

3. What are the methods of Global Routing? [D]

Sequential routing
Order-independent routing

4. What is hierarchical routing? [D]

Hierarchical routing handles all nets at a particular level at once. Rather than handling all of the nets on the chip at the same time.

5. What is Reserved-layer routing? [D]

Reserved-layer routing restricts all interconnects on each layer to flow in one direction in a given routing area.

6. What is Special Routing? [D]

The routing of nets that require special attention, clock and power nets for example, is normally done before detailed routing of signal nets.

7. List out the basic elements of the FPGA structure.(Apr 2019) [D].State the building blocks of FPGA.(Nov/Dec 2019)

The basic elements of FPGA structure are:

Logic blocks

- Based on memories *(LUT – Lookup Table)* Xilinx
- Based on multiplexers *(Multiplexers)* Actel
- Based on PAL/PLA *(PAL - Programmable Array Logic, PLA – Programmable Logic Array)* Altera
- Transistor Pairs
- Interconnection Resources
  - Symmetrical FPGA-s
- Row-based FPGA-s
- *Sea-of-gates* type of FPGA-s
- Hierarchical FPGA-s (*CPLD)*

Input-output cells (*I/O Cell)*

8. Name the elements in a Configuration Logic Block. (April 2017) [D]

Configuration Logic blocks:

- Memories *(LUT – Lookup Table, Flip-flop)* - Xilinx
- Multiplexers -Actel
- PAL/PLA *(PAL - Programmable Array Logic, PLA – Programmable Logic Array)* - Altera
- Transistor Pairs

9. Write the features of Xilinx FPGA. (April 2008) [D] (Apr2022) (Apr2021)

The features of Xilinx FPGA are:
High-performance
-5 ns pin-to-pin logic delays on all pins
Large density range - 36 to 288 macrocells with 800 to 6,400 usable gates
5 V in-systems programmable
Endurance of 10,000 program/erase cycles

10. Give the functions of Input Output Block.

The I/O Block (IOB) interfaces between the internal logic and the device user I/O pins. Each IOB includes an input buffer, output driver, output enable selection multiplexer, and user programmable ground control.

11. Write various ways of routing procedure. (Nov 2017) [D]

- Hierarchical Routing Architecture
- Island-Style Routing Architecture
- Xilinx Routing Architecture
- Altera Routing Architecture
- Actel Routing Architecture

12. What are VLSI and ULSI? (Nov 2017) [D]

Very large scale Integration (VLSI) with gates counting upto lakhs.

Ultra large-scale integration (ULSI) is the process of integrating millions of transistors on a single silicon semiconductor microchip.

13. What is programmable logic device? [D]

A programmable logic device (PLD) is an electronic component used to build reconfigurable digital circuits.

Unlike a logic gate, which has a fixed function, a PLD has an undefined function at the time of manufacture.

14. What is an antifuse? State its merits and demerits. (Nov 2016) [D]

Antifuse is nothing high resistance (>100 MΩ) is changed into low resistance(200-500Ω) by applying programming voltage.

Merit: Antifuse separate interconnect wires on the FPGA chip and the programmer blows an antifuse to make a permanent connection.

Demerit: Once an antifuse is programmed, the process can't be reversed.

15. What is PLA? [D]

Programmable logic arrays (PLAs) is a type of fixed architecture logic devices with *programmable AND gates followed by programmable OR array.*

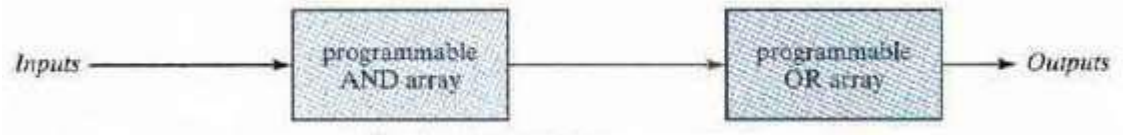


Figure: Programmable logic array

16. What is PAL? [D]

The PAL is a programmable logic device with a *fixed OR array and a programmable AND* array.

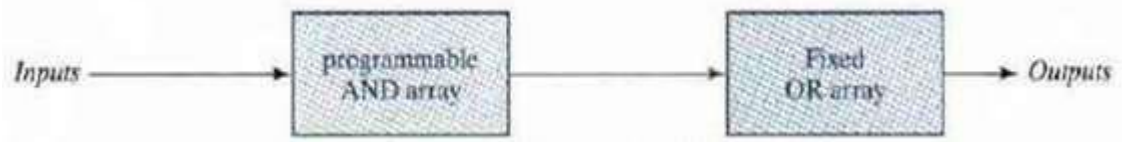


Figure: Programmable Array Logic

17. What are the types FPGA programming technologies?(or) [D]

What are the different types of programming structure available in PAL? (Nov 2008) [D]

There are three types of programming technology.

Fusible link programming (Anti fuse)
SRAM Programming
EPROM and EEPROM programming

18. What is meant by Reprogrammable Gate array (FPGA)? [D]

A field programmable gate array (FPGA) is a VLSI circuit that can be programmed at the user's location.

A typical FPGA consists of an array of millions of logic blocks, surrounded by programmable input and output blocks and connected together via programmable interconnections.

19. What is meant by configurable logic block? [D]

The programmable logic blocks of FPGAs are called Configurable Logic Blocks (CLBs).
CLBs contain LUT, FF, logic gates and Multiplexer to perform logic functions.

20. What is meant by BISTCMOS Testing? [D] Nov/Dec 2022

Testing is one of the most expensive parts of chips
– Logic verification accounts for > 50% of design effort for many chips
– Debug time after fabrication has enormous opportunity cost
– Shipping defective parts can sink a company

21. What is the need for Testing? [D]

Manufacturing test ideally would check every node in the circuit to prove it is not stuck.
Apply the smallest sequence of test vectors necessary to prove each node is not stuck.
Good observability and controllability reduces number of test vectors required for manufacturing test.
– Reduces the cost of testing
– Motivates design-for-test

22. What is Iddq testing? [D]

Iddq testing is a method for testing CMOS integrated circuits for the presence of manufacturing faults. It relies on measuring the supply current (Idd) in the quiescent state (when the circuit is not switching and inputs are held at static values).

The current consumed in the state is commonly called Iddq for Idd (quiescent) and hence the name.

23. What is the principle behind Iddq testing? [D]

Iddq testing uses the principle that in a correctly operating quiescent CMOS digital circuit, there is no static current path between the power supply and ground, except for a small amount of leakage.

Many common semiconductor manufacturing faults will cause the current to increase by orders of magnitude, which can be easily detected. This has the advantage of checking the chip for many possible faults with one measurement.

24. What are the advantages of Iddq testing? [D]

Another advantage is that it may catch faults that are not found by conventional stuck-at fault test vectors.

Iddq testing is somewhat more complex than just measuring the supply current.

It is a simple and direct test that can identify physical defects.
The area and design time overhead are very low.
Test generation is fast.
Test application time is fast since the vector sets are small.

It catches some defects that other tests, particularly stuck-at logic tests, do not.

25. What are the drawbacks of Iddq Testing? [D] (Apr2022)

Compared to scan testing, Iddq testing is time consuming, and then more expensive, since is achieved by current measurements that take much more time than reading digital pins in mass production

26. What is Design for testability?

VLSI designers have a wide variety of CAD tools to choose from, each with their own strengths and weaknesses.

27. What are the various tools available for testing? [D]

The leading Electronic Design Automation (EDA) companies include Cadence, Synopsys, Magma, and Mentor Graphics. Tanner also offers commercial VLSI design tools. The leading free tools include Electric, Magic, and LASI.

28. What are the Fault models? [D]

Numerous possible physical failures (what we are testing for) Can reduce the number of failure types by considering the effects of physical failures on the logic functional blocks: called a Assume that defects will cause the circuit to behave as if lines were "stuck" at logic 0 or 1 Most commercial tools for test are based on the "stuck-at" model Other fault models "Stuck open" model for charge retained on a CMOS node.

29. What is Observabilty and controllability? [D] Nov/Dec 2022

Observability: ease of observing a value on a node by monitoring external output pins of the chip Controllability: ease of forcing a node to 0 or 1 by driving input pins of the chip Combinational logic is usually easier to observe and control Still, NP-complete problem Finite state machines can be very difficult, requiring many cycles to enter desired state. Especially if state transition diagram is not known to the test engineer, or is too large.

30. What is Boundary scan testing? [D]

Boundary scan is a method for testing interconnects (wire lines) on printed circuit boards or sub-blocks inside an integrated circuit. Boundary scan is also widely used as a debugging method to watch integrated circuit pin states, measure voltage, or analyze sub-blocks inside an integrated circuit.

31. What are JTAG Test Operations? [D]

Devices communicate to the world via a set of input and output pins. By themselves, these pins provide limited visibility into the workings of the device. However, devices that support boundary scan contain a shift-register cell for each signal pin of the device. These registers are connected in a dedicated path around the device's boundary (hence the name).

32. **Write the test bench for and gate entity test. [D]**

```
 and2
end entity

architecture io of testand2 is
```

```
signal a,b,c:std_logic;
begin
g1:entity work.and2(ex2) port map(a,b,c)
a<=' 0' ,' 1' after 100 ns;
b<=' 0' , '1' after 150 ns;
end;
```

33. write the syntax of procedure body? [D]

Procedure procedure name (parameterlist)

34. What is test bench? [D]

A test bench is a model which is used to exercise and verify the correctness of a hardware model.

35. What are the two methods to generate stimulus values? [D]

To create waveforms and apply stimulus at discrete time intervals.
To generate stimulus based on the state of the entity or output of the entity.

36. Write notes on functionality tests? [D]

Functionality tests verify that the chip performs its intended function. These tests assert that all the gates in the chip, acting in concert, achieve a desired function. These tests are usually used early in the design cycle to verify the functionality of the circuit.

37. Write notes on manufacturing tests? [D] (Apr2021)

Manufacturing tests verify that every gate and register in the chip functions correctly. These tests are used after the chip is manufactured to verify that the silicon is intact.

38. Mention the defects that occur in a chip? [D]

Layer-to-layer shorts
Discontinuous wires
Thin-oxide shorts to substrate or well

39. Give some circuit maladies to overcome the defects? [D] (Apr2021)

a. nodes shorted to power or ground
b. nodes shorted to each other
c. inputs floating/outputs disconnected.

40. What are the different levels of design abstraction at physical design?

- Architectural or functional level
- Register Transfer-level (RTL)
- Logic level
- Circuit level

PART-B
(FIRST HALF)

1. Discuss the different types of programming technology used in FPGA design. (NOV 2016) [D]

2. Draw and explain the operation of metal-metal antifuse and EPROM transistor. (June 2012) [D]

3. Find the reason for referring EPROM technology as floating gate avalanche MOS. (Dec. 2013) [D]

4. Explain the reprogrammable device architecture with neat diagrams. [D] (OR)

With neat diagram explain the functional blocks in PDA (Programmable Device Architecture). (AU: June 2015, June 2016) [D]

5. With neat sketch explain the CLB, IOB and Programmable interconnects of an FPGA device. (May 2016) [D] (OR)

Explain about building block architecture of FPGA. (April 2017, 2018, Nov 2018) [D] (Apr 2019) **(Nov/Dec 2019) Nov/Dec 2022(Apr2021)**

6. Give short notes on FPGA interconnect routing procedures. (May 2016) [D] (Apr 2019) **(Nov/Dec 2019) (Apr2022) (Apr2021)**

PART-B
(SECOND HALF)

7. What is meant by Ad Hoc testing? Explain in detail? **[D] Nov/Dec 2022**
8. What is meant by Scan Design? Explain in detail? **[D]**
9. What is BIST? Explain in detail? **[D]**
10. Briefly explain IDDQ testing? **[D]**
11. Write short notes on Design for testability? **[D] (Apr2022) (Apr2021)**
12. Explain Boundary Scan Testing? **[D] Nov/Dec 2022**